Design and Implementation of D Flip-Flops for maximum Performance VLSI using 180nm CMOS Technology

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Abstract – This paper presents low power master slave d Flip-Flop. As these flip flop topologies have little area and low power consumption, they can be used in different applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The Flip-Flops are analyzed at 180nm technologies. The above designed Flip-Flops and Latches are compared in terms of its area, transistor count, and power dissipation. As chip manufacturing technology is suddenly on the threshold of major evaluation, which shrinks chip in size and performance is implemented in layout level which develops the low power consumption chip using recent CMOS micron layout tools. This project proposes low power design of flip flop.

Index Terms – Counter, Master Slave D flip-flop, DSCH, MicroWind.

1. INTRODUCTION

Counting is a fundamental function of digital circuits. A digital counter consists of a collection of flip-flops that change state (set or reset) in a prescribed sequence. The primary function of a counter is to produce a specified output pattern sequence. For this reason, it is also a pattern generator. This pattern sequence might correspond to the number of occurrences of an event or it might be used to control various portions of a digital system. In this latter case each pattern is associated with a distinct operation that the digital system must perform. There are tremendous applications of a counter in the digital consumer electronics market. A counter can play a vital role in several circuits ranging from a simple display to complex microcontroller circuits. Some of the apparent applications of a counter are: frequency divider in phase-locked loops, frequency synthesizers, signal generation and processing circuits, microcontrollers, digital memories and in digital clock and timing circuits. A counter is another example of a register as in the case of a register each of the 0-1 combinations that are stored in the collection of flip-flops that comprise the counter, that is the output pattern, is known as a state of the counter. The total number of states is called its modulus. Thus if a counter has „m" distinct states, then it is called a modulus-m counter or mod-m counter. The order in which the states appear is referred to as its counting sequence.

2. LITERATURE SURVEY

This paper enumerates a low power, high speed design of flip-flop having less number of transistors. In flip-flop design only one transistor is being clocked by short pulse train which is known as True Single Phase Clocking (TSPC) flip-flop. The true single-phase clock (TSPC) is common dynamic flip-flop which performs the flip-flop operation with little power and at high speeds. In this paper, an extensive comparison of existing designs of positive edge triggered True Single Phase Clocking Flip-flop is carried out. As True Single Phase Clocking (TSPC) flip-flop design has small area and low power consumption. And it can be used in various applications like digital VLSI clocking system, microprocessors, buffers etc. The analysis for various flip-flops for power dissipation and propagation delay has been carried out at different foundries. The designed flip-flops are compared in terms of power consumption and propagation delay and power delay product using DSCH and MICROWIND tools.

3. THE PROPOSED COUNTER

Master-Slave D Flip-Flop:

A master-slave D flip-flop is created by connecting two gated D latches in series and inverting the enable input to one of them. It is called master-slave because the second (slave) latch in the series only changes in response to a change in the first (master) latch. The term pulse-triggered means that data is entered on the rising edge of the clock pulse, but the output does not reflect the change until the falling edge of the clock pulse. Master-slave flip-flops can be constructed to behave as

a J-K, R-S, T or D flip-flop. The purpose of master-slave flip-flops is to protect a flip-flop's output from inadvertent changes caused by glitches on the input. Master-slave flip-flops are used in applications where glitches may be prevalent on inputs. The master-slave configuration has the advantage of being pulse-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output.

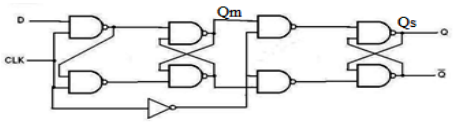


Fig-1: Master-slave D flip-flop

Fig.1 shows negative pulse-triggered master-slave D flip-flop. It responds on the negative edge of the enable input (usually a clock). The circuit consists of two D flip-flops connected together. When the clock is high, the D input is stored in the first latch, but the second latch cannot change state. When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state. The result is that output can only change state when the clock makes a transition from high to low.

4. SOFTWARE –MICROWIND

The present experiment is a guide to using the « Microwind » educational software on a PC computer. The MICROWIND program allows the student to design and simulate an integrated circuit. The package itself contains a library of common logic and analog ICs to view and simulate. MICROWIND includes all the commands for a mask editor as well as new original tools never gathered before in a single module. You can gain access to *Circuit Simulation* by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

A specific command displays the characteristics of pMOS and nMOS, where the size of the device and the process parameters can be very easily changed. Altering the MOS model parameters and, then, seeing the effects on the Vds and Ids curves constitutes a good interactive tutorial on devices.

The Process Simulator shows the layout in a vertical perspective, as when fabrication has been completed. This feature is a significant aid to supplement the descriptions of fabrication found in most textbooks.

The Logic Cell Compiler is a particularly sophisticated tool enabling the automatic design of a CMOS circuit corresponding to your logic description in VERILOG. The DSCH software, which is a user-friendly schematic editor and a logic simulator presented in a companion manual, is used to generate this Verilog description. The cell is created in compliance with the environment, design rules and fabrication specifications.

A set of CMOS processes ranging from 1.2µm down to state-of-the-art 0.25µm are proposed.

To use the MICROWIND program use the following procedure:

- Go to the directory in which the software has been copied

(The default directory is MICROWIND)

- Double-click on the Microwind icon

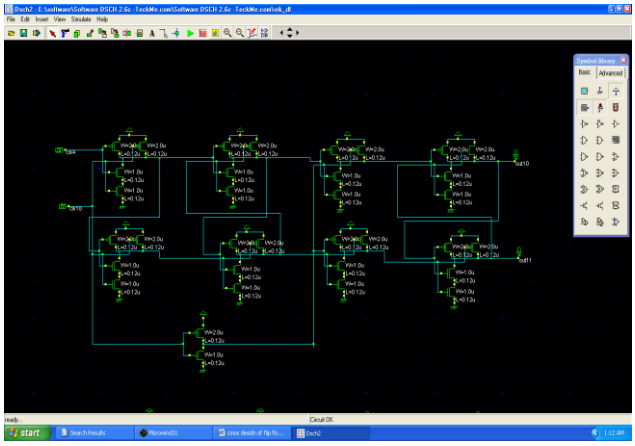
The MICROWIND display window is shown in Figure 1. It includes four main windows: the main menu, the layout displays window, the icon menu and the layer palette. The cursor appears in the middle of the layout window and is controlled by using the mouse.

The layout window features a grid that represents the current scale of the drawing, scaled in lambda units and in micron.

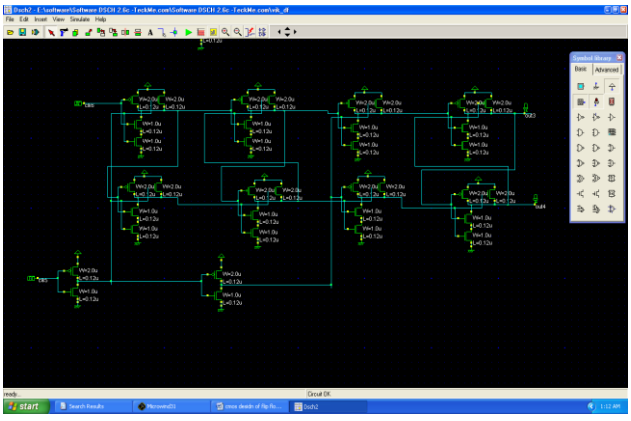
The lambda unit is fixed to half of the minimum available lithography of the technology. The default technology is a 0.8 µm technology, consequently lambda is 0.4 µm.

5. SCHEMATIC

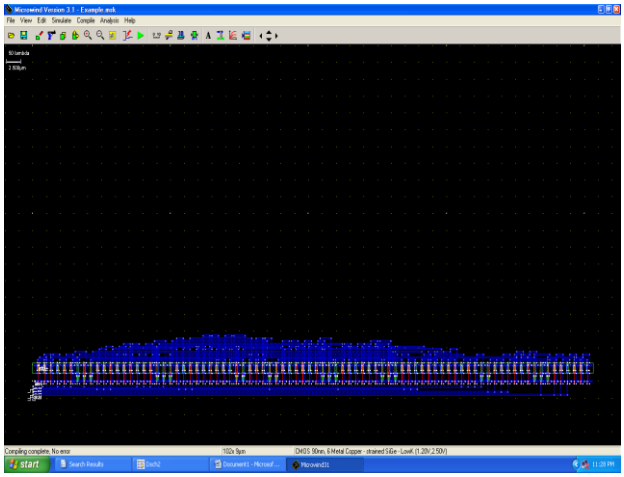
Schematic of rising edge DFF:



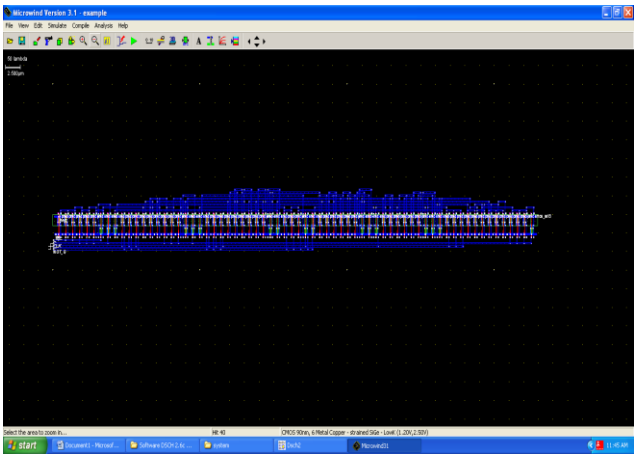
Schematic of falling edge DFF:



Layout of rising edge DFF

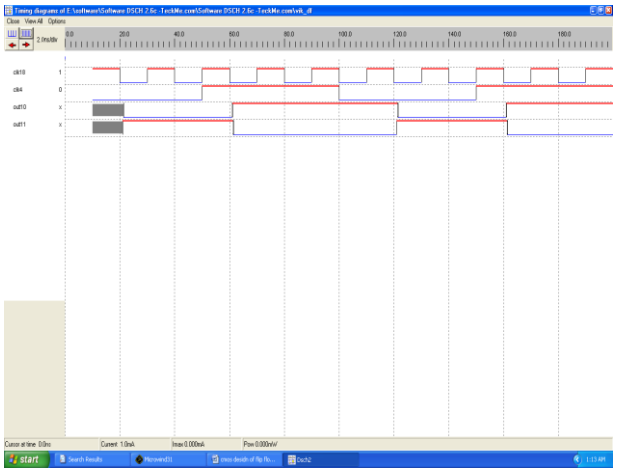


Layout of falling edge DFF:



6. SIMULATION RESULTS

Simulation result of rising edge DFF:



Simulation result of falling edge DFF:

7. CONCLUSIONS

In this paper, master slave d flip flop has been implemented. We also simulated and analyzed the master slave d flip flop. The performance of the D flip flop is analyzed in terms of area and power consumption. The main objective to minimize the power consumption. The logic and output of the master-slave D flip-flop are easily confirmed with the simulation results. Thus we present the design and implementation of master slave d flips flop which is having less area.

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